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09/911,829	07/25/2001	Tsuyoshi Tamura	110196	6319

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EXAMINER	
NGUYEN, KEVIN M	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,829	TAMURA, TSUYOSHI	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 09/10/2004 is entered. The rejections of claims 1-32 are maintained.

Double Patenting

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claims 1-32 are provisionally rejected under the judicially created doctrine of double patenting over claims 1-25 of copending Application No. 09/911,409. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows:

Claim 1 of 09/911,829 recited "a first port through which the still-image or a given command is input from an external MPU; a second port through which the moving-image data...from the external MPU" corresponding to claim 1 of 09/911,409 recited

"first and second bus line that transfer the still-image data and the moving-image data, respectively, from an external MPU."

Claim 27 of 09/911,829 recited "a first port through which the still-image data or a given command is input; a second port, independent from the first port, through which the moving-image data" corresponding to claim 1 of 09/911,409 recited "first and second independent bus lines that transfer the still-image data and the moving-image data, respectively."

Claim 28 of 09/911,829 recited "a first control circuit which controls writing or reading of the still-image data and the moving-image data that has been input separately through the first port or the second port, with respect to the RAM" corresponding to claim 21 of 09/911,409 recited "a first control circuit that controls writing or reading with respect to the RAM of the still-image data and the moving-image data that has been transferred separately over the corresponding first or second bus line, based on a given command."

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

4. Claim 27 is provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 20 of copending Application No. 09/911,409. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Identical claimed limitations as follows: claim 27 of 09/911,829 and claim 20 of 09/911,409 recited the same limitation "wherein the still-image data can be rewritten irrespective of the timing at which the moving-image data is rewritten in the RAM."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 6, 21 and 26-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kida et al (newly cited, US 6,335,728) in view of Shimamoto (previously cited, US 6,147,672).

6. As to claim 1, Kida et al teaches a memory-incorporated driver comprising:

[recited in lines 4-7 of claim 1]

SW32 a (a first port, fig. 7) through which a field memory 34A (fig. 7) for still image (fig. 9) from an external MPU defined by a data processing circuit 33 and a control circuit 32 (fig. 7);

SW32 b (a second port, fig. 7) through which a field memory 34B (fig. 7) for moving image (fig. 9) from the external MPU defined by the data processing circuit 33 and the control circuit 32 (fig. 7);

[recited in lines 10-11 of claim 1]

the field memory 34A and the field memory 34B (fig. 7) store both moving image and still image (figs. 9 and 10);

[recited in lines 12-14 of claim 1]

a memory control circuit 37 (a first control circuit, fig. 7) controls writing (WR1, WR2) or reading (RD1, RD2) of the still-image data in the field memory 34A (fig. 7) or the moving-image data in the field memory 34B (fig. 7);

[recited in lines 15-17 of claim 1]

a column driver 35 (fig. 7) and a row driver 39 (a second control circuit, fig. 7) control the display data of still image or moving image has stored in the field memories 34A and 34B (fig. 7), and drive the display panel 36 (display section, fig. 7) to display.

Accordingly, Kida et al teaches all of the claimed limitations of claim 1, except for "...which is transferred serially over a serial transfer line..." and "a reception circuit which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state."

However, Shimamoto teaches a LCD panel comprising a reception circuit (103) which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state (see figure 10, column 8, lines 58-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Kida's switch including the reception circuit (103) which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state, in view of the teaching of Shimamoto's reference because this would prevent an influence of electric wave radiation on the ambience, improve a high resolution display mode, and reduce the number of interface signal lines as taught by Shimamoto (col. 2, lines 36-41).

As to claim 6, Shimamoto teaches the serial transfer line (serial interface 206, fig. 2) is a transfer line in accordance with an LVDS standard (col. 3, lines 60-61).

As to claim 21, Kida et al discloses in Fig. 7 showing the column driver 35 (a plurality of first electrodes, fig. 7) and the row driver 39 (a plurality of second electrodes, fig. 7) drive the display panel 36 (a panel, fig. 7). The field memories 34A and 34B (fig. 7) drive the column driver 35 (a plurality of first electrodes, fig. 7). The row driver 39 drives the plurality of second electrodes of the display panel 36.

As to claim 26, Kida et al teaches the microprocessor unit including said data processing circuit 33 (fig. 7) and said control circuit 32 (fig. 7) which supply the command from the operating means 38 (fig. 7) the still image data, and the moving image data to the display unit 36 (fig. 7).

7. As to claim 27, Kida et al teaches a memory-incorporated driver comprising:

[recited in lines 3-6 of claim 27]

SW32 a (a first port, fig. 7) through which a field memory 34A (fig. 7) for still image (fig. 9) or a given command of operating means 38 (fig. 7) is input;

SW32 b (a second port, fig. 7) through which a field memory 34B (fig. 7) for moving image (fig. 10);

[recited in lines 9-10 of claim 27]

the field memory 34A and the field memory 34B (a RAM, fig. 7) store both moving image and still image (fig. 9);

[recited in lines 11-13 of claim 27]

a memory control circuit 37 (a first control circuit, fig. 7) controls writing (WR1, WR2) or reading (RD1, RD2) of the still-image data in the field memory 34A (fig. 7) or the moving-image data in the field memory 34B (fig. 7);

[recited in lines 14-16 of claim 27]

a column driver 35 (fig. 7) and a row driver 39 (a second control circuit, fig. 7) control the display data of still image or moving image has stored in the field memories 34A and 34B (fig. 7), and drive the display panel 36 (display section, fig. 7) to display.

[recited in lines 17-18 of claim 27]

Fig. 8C discloses still image writing mode can be rewritten (see col. 20, lines 17-20) at time t2 to t4 (fig. 8N) irrespective of the timing at t0 to t2 (fig. 8N) which the moving-image data is rewritten (see col. 20, lines 17-20) in the first memory 34A and second memory 34B (the RAM, fig. 7).

Accordingly, Kida et al teaches all of the claimed limitations of claim 1, except for "...which is transferred serially over a serial transfer line..." and "a reception circuit which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state."

However, Shimamoto teaches a LCD panel comprising a reception circuit (103) which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state (see figure 10, column 8, lines 58-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Kida's switch including the reception circuit (103) which differentially amplifies the differential signal input from the second port and

creates the moving image data in a parallel state, in view of the teaching of Shimamoto's reference because this would prevent an influence of electric wave radiation on the ambience, improve a high resolution display mode, and reduce the number of interface signal lines as taught by Shimamoto (col. 2, lines 36-41).

8. As to claim 28, Kida et al teaches a memory-incorporated driver comprising:

[recited in lines 3-6 of claim 28]

SW32 a (a first port, fig. 7) through which a field memory 34A (fig. 7) for still image (fig. 9) or a given command of operating means 38 (fig. 7) is input;

SW32 b (a second port, fig. 7) through which a field memory 34B (fig. 7) for moving image (fig. 10);

[recited in lines 9-10 of claim 28]

the field memory 34A and the field memory 34B (a RAM, fig. 7) store both moving image and still image (fig. 9);

[recited in lines 11-13 of claim 28]

a memory control circuit 37 (a first control circuit, fig. 7) controls writing (WR1, WR2) or reading (RD1, RD2) of the still-image data and (emphasis) the moving-image data in the field memories 34A and 35B (fig. 8C and fig. 8N, the motion image/still image mixture display mode, see col. 13, lines 44-50);

[recited in lines 14-16 of claim 28]

a column driver 35 (fig. 7) and a row driver 39 (a second control circuit, fig. 7) control the display data of still image or moving image has stored in the field memories 34A and 34B (fig. 7), and drive the display panel 36 (display section, fig. 7) to display.

Accordingly, Kida et al teaches all of the claimed limitations of claim 1, except for "...which is transferred serially over a serial transfer line..." and "a reception circuit which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state."

However, Shimamoto teaches a LCD panel comprising a reception circuit (103) which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state (see figure 10, column 8, lines 58-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Kida's switch including the reception circuit (103) which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state, in view of the teaching of Shimamoto's reference because this would prevent an influence of electric wave radiation on the ambience, improve a high resolution display mode, and reduce the number of interface signal lines as taught by Shimamoto (col. 2, lines 36-41).

As to claims 29, 30, Kida et al discloses in Fig. 7 showing the column driver 35 (a plurality of first electrodes, fig. 7) and the row driver 39 (a plurality of second electrodes, fig. 7) drive the display panel 36 (a panel, fig. 7). The field memories 34A and 34B (fig. 7) drive the column driver 35 (a plurality of first electrodes, fig. 7).

As to claims 31, 32, Kida et al teaches the microprocessor unit including said data processing circuit 33 (fig. 7) and said control circuit 32 (fig. 7) which supply the command from the operating means 38 (fig. 7) the still image data, and the moving image data to the display unit 36 (fig. 7).

9. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kida et al and Shimamoto, and further in view of Silverman et al (previously cited, US 6,370,603).

As to claims 11 and 16, Kida et al and Shimamoto teach all of the claimed limitations of claim 1, except for the serial transfer line is a transfer line in accordance with a USB standard and an IEEE 1394 standard.

However, Silverman et al teaches the serial transfer line is a transfer line (serial interface engine 206, fig. 2) in accordance with a USB standard and an IEEE 1394 standard (column 8, lines 19-23).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Kida's switch including the serial transfer line is a transfer line in accordance with a USB standard and an IEEE 1394 standard, in view of the teaching of Silverman's reference because this would provide an improved technique for effecting digital communications between digital devices and system using different communication protocols as taught by Silverman (column 4, lines 10-13).

10. Claims 2-5, 7-10 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kida et al and Shimamoto as applied to claim 1 above, and further in view of Chida (previously cited, US 6,313,863).

As to claim 2, Kida et al and Shimamoto teach all of the claimed limitations of claim 1, except for a data validation signal generation circuit.

However, Chida teaches a halt control circuit (a system control unit 26, fig. 1). A validity table 26-1 manages validities of each image block designated by a validity

designating unit 36. A special coded data table 26-2 manages a special coded image. A static image table 26-3 manages a static image. A validity designating unit 34 designates validities of each block of an image in accordance with instructions from the system control unit 26 that controls a control unit 34 based on the validity table 26-1(fig. 1, col. 4, lines 23-30).

Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Shimamoto's reception circuit including a data validation signal generation circuit, in view of the teaching of Chida's reference because this would improve the quality of an image that is transmitted through a communication channel or line, and improve a quality image in an acceptable amount of time from a partner's terminal as taught by Chida (col. 2, lines 40-45).

As to claims 3-5, Chida teaches when the receiving side displays only the valid area, the system control unit 26 of the receiving side controls the synthesizing/ processing unit 125 so that unit 125 extracts a part of the image stored in the receiving video RAM 121 based on the validity information of the blocks (fig. 11a, col. 9, lines 48-52).

As to claims 7-10, Shimamoto teaches the serial transfer line is a transfer line in accordance with an LVDS standard (col. 3, lines 60-61).

As to claims 22-25, Kido discloses in Fig. 7 showing the column driver 35 (a plurality of first electrodes, fig. 7) and the row driver 39 (a plurality of second electrodes, fig. 7) drive the display panel 36 (a panel, fig. 7). The field memories 34A and 34B (fig.

7) drive the column driver 35 (a plurality of first electrodes, fig. 7). The row driver 39 drives the plurality of second electrodes of the display panel 36.

11. Claims 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kida et al and Shimamoto, and further in view of Silverman et al.

As to claims 12-20, Kida et al and Shimamoto teach all of the claimed limitations of claim 1, except for the serial transfer line is a transfer line in accordance with a USB standard and an IEEE 1394 standard.

However, Silverman et al teaches the serial transfer line (serial interface engine 206, fig. 2) is a transfer line in accordance with a USB standard and an IEEE 1394 standard (column 8, lines 19-23).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Kida's switch including the serial transfer line is a transfer line in accordance with a USB standard and an IEEE 1394 standard, in view of the teaching of Silverman's reference because this would provide an improved technique for effecting digital communications between digital devices and system using different communication protocols as taught by Silverman et al (column 4, lines 10-13).

Response to Arguments

12. Applicant's arguments filed 09/10/2004 have been fully considered but they are not persuasive. Applicant argues feature at pages 9 and 12 in the independent claims 1, 27, 28 that are newly recited. Thus, new grounds of rejection have been used. See above rejections.

13. In response to applicant's argument at page 10 that claim 26 recites "the MPU which supplies the command, the still-image data, and the moving-image data to the display unit." This argument is not persuasive because Kida teaches the microprocessor unit including said data processing circuit 33 (fig. 7) and said control circuit 32 (fig. 7) which supply the command from the operating means 38 (fig. 7) the still image data, and the moving image data to the display unit 36 (fig. 7).

14. In response to applicant's argument at page 11 that claims 3-5, 8-10 and 23-28 recite "wherein the validation signal is used as a synchronization signal that synchronizes the writing of the moving-image data in the RAM." This argument is not persuasive because Fig. 11(a) of Chida shows an image data "arrow" (the hatching image data captures from the camera 10 (fig. 11a) which defines the motion image) that synchronizes the validity information of blocks "arrow" (the first is that the plural sources a, b, c (fig. 15b) transmit image data in response to a common synchronizing signal, see fig. 15(b), col. 12, lines 32-34).

Fore these reasons, the rejection based on Kida et al, Shimamoto, Silverman et al, Chida have been maintained.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KN
November 24, 2004

XIAO WU
PRIMARY EXAMINER